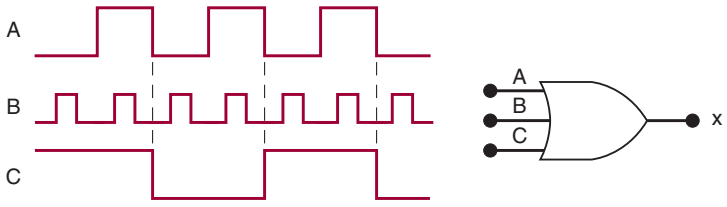
SECTION 3-3

B 3-1.* (a) Draw the output waveform for the OR gate of Figure 3-52.

B (b) Suppose that the *A* input in Figure 3-52 is unintentionally shorted to ground (i.e., $A = 0$). Draw the resulting output waveform.

B (c) Suppose that the *A* input in Figure 3-52 is unintentionally shorted to the +5 V supply line (i.e., $A = 1$). Draw the resulting output waveform.

FIGURE 3-52



3-2. A three-input OR gate should be producing a logic 0 at its output but instead it is producing a logic 1. How can you determine which of the three inputs is incorrect?

C 3-3. Read the statements below concerning an OR gate. At first, they may appear to be valid, but after some thought you should realize that neither one is *always* true. Prove this by showing a specific example to refute each statement.

(a) If the output waveform from an OR gate is the same as the waveform at one of its inputs, the other input is being held permanently LOW.

(b) If the output waveform from an OR gate is always HIGH, one of its inputs is being held permanently HIGH.

B 3-4. How many different sets of input conditions will produce a HIGH output from a five-input OR gate?

SECTION 3-4

3-5. A three-input AND gate should be producing a logic 1 at its output but instead it is producing a logic 0. How can you determine which of the three inputs is incorrect?

B 3-6. Change the OR gate in Figure 3-52 to an AND gate.

(a)*Draw the output waveform.

(b) Draw the output waveform if the *A* input is permanently shorted to ground.

(c) Draw the output waveform if *A* is permanently shorted to +5 V.

D 3-7.* Refer to Figure 3-4. Modify the circuit so that the alarm is to be activated only when the pressure and the temperature exceed their maximum limits at the same time.

B 3-8.* Change the OR gate in Figure 3-6 to an AND gate and draw the output waveform.

B 3-9. Suppose that you have an unknown two-input gate that is either an OR gate or an AND gate. What combination of input levels should you apply to the gate's inputs to determine which type of gate it is?

*Answers to problems marked with an asterisk can be found in the back of the text.

B 3-10. *True or false:* No matter how many inputs it has, an AND gate will produce a HIGH output for only one combination of input levels.

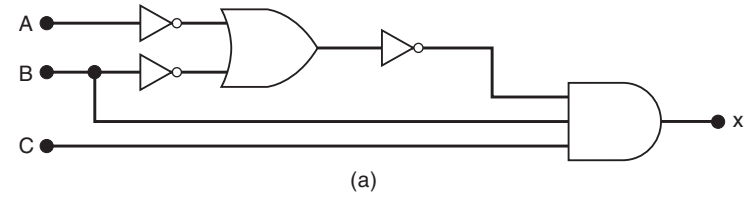
SECTIONS 3-5 TO 3-7

B 3-11. Apply the *A* waveform from Figure 3-23 to the input of an INVERTER. Draw the output waveform. Repeat for waveform *B*.

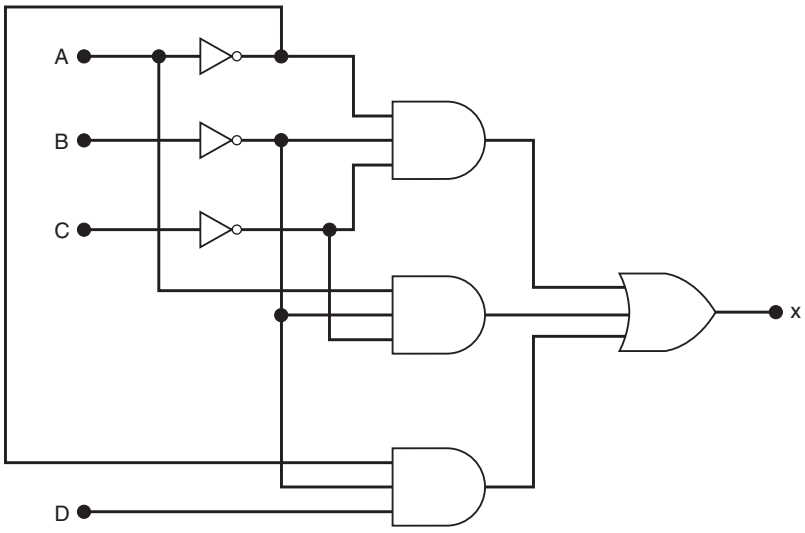
B 3-12. (a)* Write the Boolean expression for output x in Figure 3-53(a). Determine the value of x for all possible input conditions, and list the values in a truth table.

(b) Repeat for the circuit in Figure 3-53(b).

FIGURE 3-53



(a)



(b)

B 3-13.* Create a complete analysis table for the circuit of Figure 3-15(b) by finding the logic levels present at each gate output for each of the 32 possible input combinations.

B 3-14. (a)*Change each OR to an AND, and each AND to an OR, in Figure 3-15(b). Then write the expression for the output.

(b) Complete an analysis table.

B 3-15. Create a complete analysis table for the circuit in Figure 3-15(a) by finding the logic levels present at each gate output for each of the 16 possible input combinations.

SECTION 3-8

B 3-16. For each of the following expressions, construct the corresponding logic circuit, using AND and OR gates and INVERTERs.

(a)* $x = \overline{AB(C + D)}$

(b)* $z = \overline{A + B + \overline{C}D\overline{E})} + \overline{B}C\overline{D}$

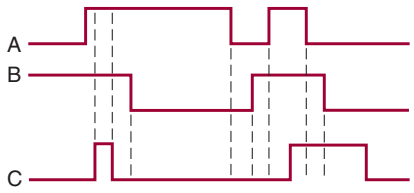
(c) $y = (\overline{M + N} + \overline{P}Q)$

(d) $x = \overline{W + P\overline{Q}}$
(e) $z = MN(P + \overline{N})$
(f) $x = (A + B)(\overline{A} + \overline{B})$
(g) $g = AC + B\overline{C}$
(h) $h = \overline{\overline{AB} + \overline{CD}}$

SECTION 3-9

B 3-17.*(a) Apply the input waveforms of Figure 3-54 to a NOR gate, and draw the output waveform.
(b) Repeat with C held permanently LOW.
(c) Repeat with C held HIGH.

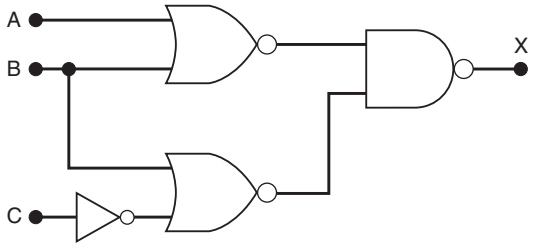
FIGURE 3-54



B 3-18. Repeat Problem 3-17 for a NAND gate.

C 3-19.*Write the expression for the output of Figure 3-55, and use it to determine the complete truth table. Then apply the waveforms of Figure 3-54 to the circuit inputs, and draw the resulting output waveform.

FIGURE 3-55



B 3-20. Determine the truth table for the circuit of Figure 3-24.

B 3-21. Modify the circuits that were constructed in Problem 3-16 so that NAND gates and NOR gates are used wherever appropriate.

SECTION 3-10

C 3-22. Prove theorems (15a) and (15b) by trying all possible cases.

B 3-23.*DRILL QUESTION
Complete each expression.

(a) $A + 1 =$ _____
(b) $A \cdot A =$ _____
(c) $B \cdot \overline{B} =$ _____
(d) $C + C =$ _____
(e) $x \cdot 0 =$ _____
(f) $D \cdot 1 =$ _____
(g) $D + 0 =$ _____
(h) $C + \overline{C} =$ _____
(i) $G + GF =$ _____
(j) $y + \overline{w}y =$ _____

C 3-24. (a)*Simplify the following expression using theorems (13b), (3), and (4):

$$x = (M + N)(\overline{M} + P)(\overline{N} + \overline{P})$$

(b) Simplify the following expression using theorems (13a), (8), and (6):

$$z = \overline{A}B\overline{C} + AB\overline{C} + B\overline{C}D$$

SECTIONS 3-11 AND 3-12

C 3-25. Prove DeMorgan's theorems by trying all possible cases.

B 3-26. Simplify each of the following expressions using DeMorgan's theorems.

(a)* $\overline{\overline{A}B\overline{C}}$
(b) $\overline{\overline{A} + \overline{B}C}$
(c)* $\overline{AB\overline{C}\overline{D}}$
(d) $\overline{A + \overline{B}}$
(e)* $\overline{\overline{A}\overline{B}}$
(f) $\overline{\overline{A} + \overline{C} + \overline{D}}$
(g)* $\overline{A(\overline{B + \overline{C}})D}$
(h) $\overline{(M + \overline{N})(\overline{M} + N)}$
(i) $\overline{\overline{\overline{A}B\overline{C}D}}$

B 3-27.*Use DeMorgan's theorems to simplify the expression for the output of Figure 3-55.

C 3-28. Convert the circuit of Figure 3-53(b) to one using only NAND gates. Then write the output expression for the new circuit, simplify it using DeMorgan's theorems, and compare it with the expression for the original circuit.

C 3-29. Convert the circuit of Figure 3-53(a) to one using only NOR gates. Then write the expression for the new circuit, simplify it using DeMorgan's theorems, and compare it with the expression for the original circuit.

B 3-30. Show how a two-input NAND gate can be constructed from two-input NOR gates.

B 3-31. Show how a two-input NOR gate can be constructed from two-input NAND gates.

C 3-32. A jet aircraft employs a system for monitoring the rpm, pressure, and temperature values of its engines using sensors that operate as follows:

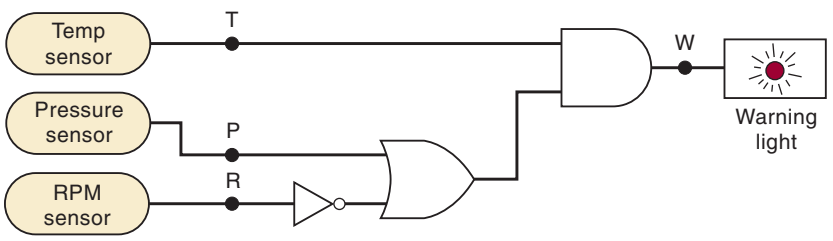
$$RPM \text{ sensor output} = 0 \text{ only when speed} < 4800 \text{ rpm}$$
$$P \text{ sensor output} = 0 \text{ only when pressure} < 220 \text{ psi}$$
$$T \text{ sensor output} = 0 \text{ only when temperature} < 200^\circ \text{F}$$

Figure 3-56 shows the logic circuit that controls a cockpit warning light for certain combinations of engine conditions. Assume that a HIGH at output W activates the warning light.

(a)*Determine what engine conditions will give a warning to the pilot.

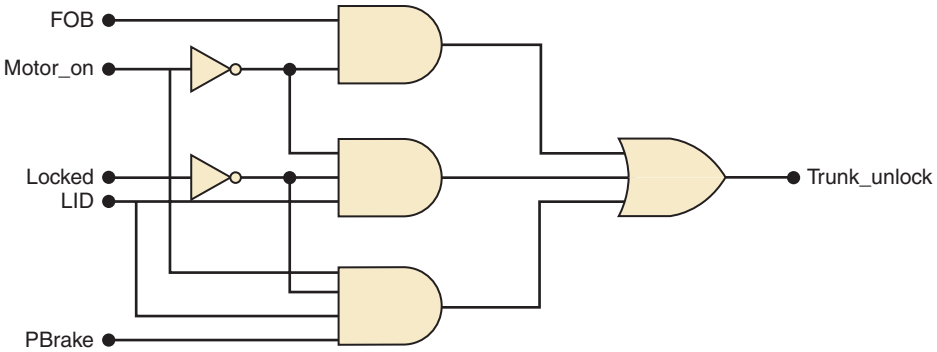
(b) Change this circuit to one using all NAND gates.

FIGURE 3-56



3-33. The trunk of an automobile is opened in one of two ways: by pressing a button on the trunk lid or by pressing the trunk button on the key fob. However, these buttons only open the trunk under certain conditions for safety and security purposes. The logic diagram for this circuit is shown in Figure 3-57.

FIGURE 3-57



The output is Trunk_unlock

HIGH activates the latch release and opens the trunk.

The inputs are defined as follows:

Button on trunk lid	LID	LOW = not pressed	HIGH = pressed
Button on key fob	FOB	LOW = not pressed	HIGH = pressed
Condition of door locks	Locked	Low = unlocked	HIGH = locked
Parking brake	PBrake	Low = not set (off)	HIGH = brake set
Engine status	Motor_on	Low = off	HIGH = motor on

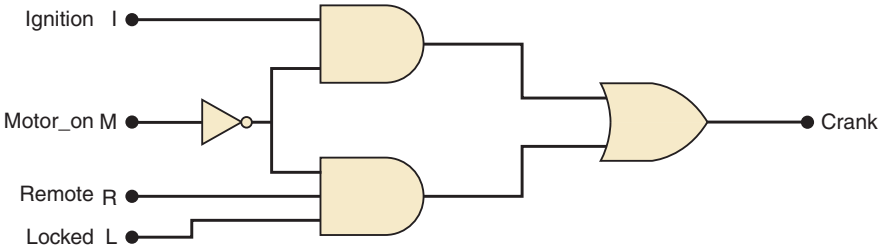
(a) Write the conditions in English that will open the trunk.

(b) Write the Boolean equation using the signal names given.

(c) Redraw the circuit using all NAND gates (assume you have up to four-input NAND gates available).

3-34. The remote start for an automobile will crank the engine under certain conditions. The logic circuit is shown in Figure 3-58. Inputs are defined as follows:

FIGURE 3-58



I	Ignition	Ignition switch in START position = HIGH
M	Motor_on	Engine running = HIGH
R	Remote	Remote start button on FOB pressed = HIGH
L	Locked	Doors locked = HIGH

(a) Write the Boolean expression from the circuit diagram.

(b) Draw the truth table for this circuit.

(c) Write the unsimplified SOP expression (using all four-variable product terms).

(d) Use Boolean algebra to simplify the SOP expression in (c) to match the expression in (a)

(e) Implement this circuit using only NAND gates.

SECTIONS 3-13 AND 3-14

B 3-35.* For each statement below, draw the appropriate logic-gate symbol—standard or alternate—for the given operation.

(a) A HIGH output occurs only when all three inputs are LOW.

(b) A LOW output occurs when any of the four inputs is LOW.

(c) A LOW output occurs only when all eight inputs are HIGH.

B 3-36. Draw the standard representations for each of the basic logic gates. Then draw the alternate representations.

C 3-37. The circuit of Figure 3-55 is supposed to be a simple digital combination lock whose output will generate an active-LOW $\overline{UNLOCK}$ signal for only one combination of inputs.

(a)*Modify the circuit diagram so that it represents more effectively the circuit operation.

(b) Use the new circuit diagram to determine the input combination that will activate the output. Do this by working back from the output using the information given by the gate symbols, as was done in Examples 3-22 and 3-23. Compare the results with the truth table obtained in Problem 3-19.

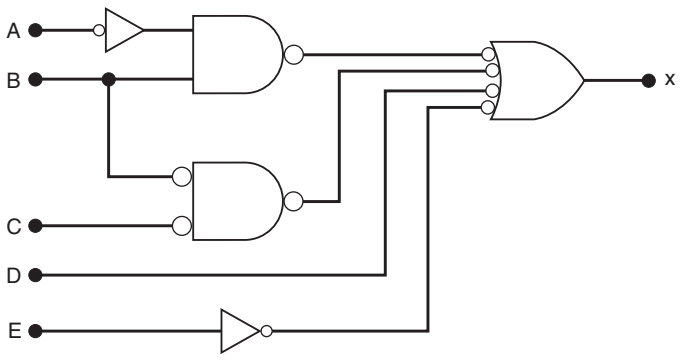
C 3-38. (a) Determine the input conditions needed to activate output Z in Figure 3-37(b). Do this by working back from the output, as was done in Examples 3-22 and 3-23.

(b) Assume that it is the LOW state of Z that is to activate the alarm. Change the circuit diagram to reflect this, and then use the revised diagram to determine the input conditions needed to activate the alarm.

D 3-39. Modify the circuit of Figure 3-40 so that $A_1 = 0$ is needed to produce $LCD = 1$ instead of $A_1 = 1$.

B 3-40.*Determine the input conditions needed to cause the output in Figure 3-59 to go to its active state.

FIGURE 3-59



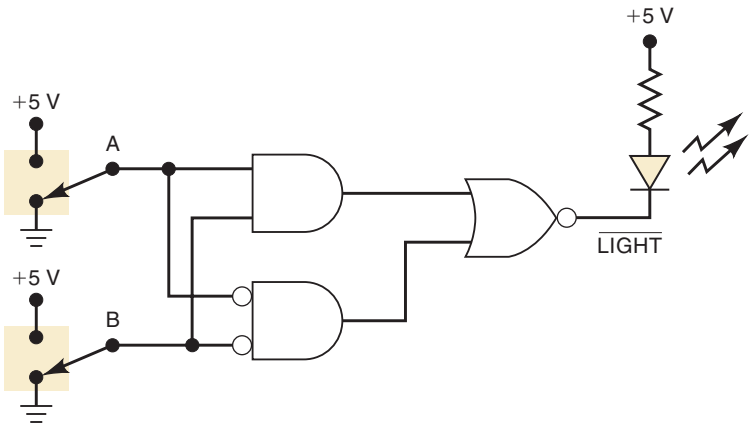
B 3-41.*(a) What is the asserted state for the output of Figure 3-59?

(b) What is the asserted state for the output of Figure 3-36(c)?

B 3-42. Use the results of Problem 3-40 to obtain the complete truth table for the circuit of Figure 3-59.

N 3-43.* Figure 3-60 shows an application of logic gates that simulates a two-way switch like the ones used in our homes to turn a light on or off from two different switches. Here the light is an LED that will be ON (conducting) when the NOR gate output is LOW. Note that this output is labeled $\overline{LIGHT}$ to indicate that it is active-LOW. Determine the input conditions needed to turn on the LED. Then verify that the circuit operates as a two-way switch using switches *A* and *B*. (In Chapter 4, you will learn how to design circuits like this one to produce a given relationship between inputs and outputs.)

FIGURE 3-60



SECTION 3-15

B 3-44. A 7406 TTL inverter has a maximum t_{PLH} of 15 ns and a t_{PHL} of 23 ns. A positive pulse that lasts 100 ns is applied to the input.

(a) Draw the input and output waveforms. Scale the X-axis such that the end time is 200 ns.

(b) Label t_{PLH} and t_{PHL} on the graph.

(c) What is the pulse width of the output if worst case propagation delays occur?

SECTION 3-17
HDL DRILL QUESTIONS

H 3-45.* *True or false:*

(a) VHDL is a computer programming language.

(b) VHDL can accomplish the same thing as AHDL.

(c) AHDL is an IEEE standard language.

(d) Each intersection in a switch matrix can be programmed as an open or short circuit between a row and column wire.

(e) The first item that appears at the top of an HDL listing is the functional description.

(f) The type of an object indicates if it is an input or an output.

(g) The mode of an object determines if it is an input or an output.

(h) Buried nodes are nodes that have been deleted and will never be used again.

(i) Local signals are another name for intermediate variables.

(j) The header is a block of comments that document vital information about the project.

SECTION 3-18

B 3-46. Redraw the programmable connection matrix from Figure 3-44. Label the output signals (horizontal lines) from the connection matrix (from top row to bottom row) as follows: AAABADHE. Draw an X in the appropriate intersections to short-circuit a row to a column and create these connections to the logic circuit.

H 3-47.* Write the HDL code in the language of your choice that will produce the following output functions:

$$X = A + B$$
$$Y = \overline{AB}$$
$$Z = A + B + C$$

H 3-48. Write the HDL code in the language of your choice that will implement the logic circuit of Figure 3-39.

(a) Use a single Boolean equation.

(b) Use the intermediate variables V, W, X, and Y.

MICROCOMPUTER APPLICATION

C 3-49.* Refer to Figure 3-40 in Example 3-23. Inputs A_7 through A_0 are *address* inputs that are supplied to this circuit from outputs of the microprocessor chip in a microcomputer. The eight-bit address code A_7 to A_0 selects which device the microprocessor wants to activate. In Example 3-23, the required address code to activate the LCD was A_7 through $A_0 = 11111110_2 = FE_{16}$.

Modify the circuit so that the microprocessor must supply an address code of $4A_{16}$ to activate the LCD.

CHALLENGING EXERCISES

C 3-50. Show how $x = AB\overline{C}$ can be implemented with one two-input NOR and one two-input NAND gate.

C 3-51.* Implement $y = ABCD$ using only two-input NAND gates.

ANSWERS TO OUTCOME ASSESSMENT QUESTIONS

SECTION 3-1

1. Constant; GND 2. Variables; A, B 3. See glossary

SECTION 3-2

1. $x = 1$ 2. $x = 0$ 3. 32

SECTION 3-3

1. All inputs LOW. 2. $x = A + B + C + D + E + F$ 3. Constant HIGH.

SECTION 3-4

1. All five inputs = 1. 2. A LOW input will keep the output LOW. 3. False; see truth table of each gate.

SECTION 3-5

1. Output of second INVERTER will be the same as input A. 2. y will be LOW only for $A = B = 1$.

SECTION 3-6

1. $x = \overline{A} + B + C + \overline{AD}$ 2. $x = D(\overline{AB + C}) + E$

SECTION 3-7

1. $x = 1$ 2. $x = 1$ 3. $x = 1$ for both.

SECTION 3-8

1. See Figure 3-15(a). 2. See Figure 3-17(b). 3. See Figure 3-15(b).

SECTION 3-9

1. All inputs LOW. 2. $x = 0$ 3. $x = \overline{A + B + \overline{CD}}$

SECTION 3-10

1. $y = A\overline{C}$ 2. $y = \overline{A}\,\overline{B}\,\overline{D}$ 3. $y = \overline{A}D + BD$

SECTION 3-11

1. $z = \overline{A}\,\overline{B} + C$ 2. $y = (\overline{R} + S + \overline{T})Q$ 3. Same as Figure 3-28 except NAND is replaced by NOR. 4. $y = \overline{A}B(C + \overline{D})$

SECTION 3-12

1. Three. 2. NOR circuit is more efficient because it can be implemented with only three NOR gates. 3. $x = \overline{(\overline{AB})(\overline{CD})} = \overline{\overline{AB}} + \overline{(\overline{CD})} = AB + CD$ 4. 3 5. 1

SECTION 3-13

1. Output goes LOW when any input is HIGH. 2. Output goes HIGH only when all inputs are LOW. 3. Output goes LOW when any input is LOW. 4. Output goes HIGH only when all inputs are HIGH.

SECTION 3-14

1. Z will go HIGH when $A = B = 0$ and $C = D = 1$ 2. Z will go LOW when $A = B = 0$, $E = 1$, and either C or D or both are 0. 3. Two 4. Two 5. LOW 6. $A = B = 0$, $C = D = 1$ 7. $\overline{W}$

SECTION 3-15

1. The time scale is in nanoseconds and it takes a finite amount of time to change states. 2. From 50% point on the input to 50% point on the output 3. t_{PHL} 4. t_{PLH}

SECTION 3-16

1. Boolean equation, truth table, logic diagram, timing diagram, language.
2. Schematic entry of .bdf files and simulation using timing diagrams.

SECTION 3-17

1. Hardware description language 2. To describe a digital circuit and its operation. 3. To give a computer a sequential list of tasks. 4. HDL describes concurrent hardware circuits; computer instructions execute one at a time. 5. Altera Corporation. 6. U.S. Dept. of Defense.

SECTION 3-18

1. Programmable logic device. 2. By making and breaking connections in a switching matrix. 3. It translates HDL code into a pattern of bits to configure the switching matrix.

SECTION 3-19

AHDL

1. The input and output definitions. 2. The description of how it operates.

VHDL

1. To give a name to the circuit and define its inputs and outputs. 2. The ARCHITECTURE description. 3. <=

SECTION 3-20

AHDL

1. NODE 2. After the I/O definition and before BEGIN. 3. No 4. % 5. --

VHDL

1. SIGNAL 2. Inside ARCHITECTURE before BEGIN. 3. No 4. --